

REMARKS

With the above amendments, claims 3, 7 and 8 have been amended to delete the multiple dependencies and make those claims singly dependent on claim 1.

A marked-up version showing the changes made to the claims is attached for the convenience of the Examiner. No new matter has been added by the above amendments.

In view of the above, it is believed that the application is now in good condition for examination. Questions are welcomed by the below-signed attorney for applicant.

Respectfully submitted,

GRiffin & Szipl, PC


Szipl, Joerg Uwe
Reg. No. 31,799

GRiffin & Szipl, PC
Suite PH-1
2300 Ninth Street, South
Arlington, VA 22204

Telephone: (703) 979-5700
Facsimile: (703) 979-7429
Customer No.: 24203

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

3. (Amended) The computer architecture according to claim 1-~~or 2~~, wherein each of said memory modules receives a synchronization signal for achieving synchronization with the CPU module and other memory modules, and it is constituted such that it comprises input that is connectable to any of said plurality of sets of buses, and output that is connectable to any other of said plurality of sets of buses, and at least, it is able to output data according to said synchronization signal by connecting the input to one of said buses, inputting data and connecting the output to any of said other buses.

7. (Amended) The computer architecture according to any one of claims 1 through ~~6~~ claim 1, wherein, when said processor receives an instruction to delete a specific element within a series of data, insert a specific element into said series of data, or add a specific element to the end of a series of data, said processor performs a table lookup, compares the region of data that it manages itself against the position of said element subject to deletion, insertion or addition, and based on the results of said comparison, updates the content of said table.

8. (Amended) The computer architecture according to any one of claims 1 through ~~7~~ claim 1, wherein, in response to a given instruction, said processor converts subscripts for specifying elements within a series of data, and/or executes value conversion for giving a specific modification to elements.